32. (Twice amended) A trench DMOS transistor cell, comprising:

a substrate;

an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having substantially vertical side walls and having a predetermined depth d_{tr}; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max},

wherein the depth d_{tr} is less than the depth d_{max}, and

wherein [the difference between the depth d_{max} and the depth d_{tr} is sufficient to force] junction breakdown occurs away from the trench and into the epitaxial layer.

54. (Twice amended) A semiconductor device comprising:

a semiconductor [substrate] structure having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor [substrate] structure including a drain region, a source region, a body region, and a gate region within said trench and separated from said body region by a dielectric material, said body region having a maximum depth of d_{max}, wherein said maximum depth d_{max} being greater than said depth d_{tr} [by an amount sufficiently large to force] and wherein junction breakdown occurs away from said trench.

REMARKS

Claims 17-42, 44 and 46-65 were pending prior to the present amendment. Claims 17, 30, 32, 54 and 58 are amended. Claim 24 is cancelled.

The Examiner objected to the Figures under 37 C.F.R. § 1.83(a), stating that the figures do not show a recited feature required by twice amended Claim 30. As amended, Applicants

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believe that Claim 30 fully complies with the 37 C.F.R. § 1.83(a).

The Examiner rejected Claims 30, 31, 55-58 and 59 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner objected to Claims 30 and 58 on antecedent basis grounds. The Examiner rejected Claim 55 based on the apparent requirement of two different "substrates". The Examiner rejected Claims 31, 56-57 and 59 based on their respective dependence on rejected base claims. Applicants believe that the deficiency in the rejected claims are corrected in Applicants' amendments of Claims 30, 54 and 58 above.

The Examiner maintained his previous rejections of:

(i) Claims 17-22, 24-37, 44, 46-49, 51-58, and 64-65 under 35 U.S.C. 103 as unpatentable over considerations of Tonnel and Ueda et al.;

(ii) Claim 50 under 35 U.S.C. 103 as unpatentable over considerations of Tonnel, Ueda et al. and Lisiak et al.;

(iii) Claims 39, 40, 41, 60, 61 and 62 under 35 U.S.C. § 103, as unpatentable over considerations of Tonnel, Ueda et al. and Yamabe et al.; and

(iv) Claims 17-42, 44 and 46-65 under the judicially established doctrine of obviousness-type double patenting as unpatentable over Patent Claim 2 and its dependent Claims in US 5,072,266, but further considered with Tonnel, Lisiak et al., Ueda et al. and Yamabe et al. teaching that the differences between the claimed subject matters would have been obvious.

With respect to Applicants arguments of September 30, 1996, the Examiner states:

> Among other things, in response, we are unable to understand the Applicants' fortuitous characterization. From the Applicants point of view, how fortuitous can it be not to possess another US Patent claiming unobvious subject matter based upon the originally filed disclosure due to the Tonnel prior art? From our point of

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> view, we found no fortune in searching for and first applying Tonnel in June 1994, Paper No. 8, and yet, in 1997, unsuccessfully convincing the Applicants that the presently claimed combination was evidently envisaged by Tonnel. Further, we have considered the Tonnel disclosure as a whole, not merely Figwes 3, 12 and 19 as alleged. We provided a more careful analysis of Tonnel in Paper No. 12 wherein, on pages 4 and 5, we found that Figures 4 through 12, combined with the corresponding written disclosure, plausibly demonstrated that deep base regions (22), first introduced in the process step of Figure 4, plausibly grew deeper during the thermal oxidation step of Figure 5, at about the same depth as grooves (30) of Figure 6, and plausibly grew still further deeper than the depth of the grooves during ion implantation and annealing steps subsequently performed in the process steps of Figures 9 and 10, to yield a device shown with Figure 12 that obviously possesses all the claimed characteristics. The Applicants have provided no meaningful counter-analysis from which we could plausibly conclude that our analysis was essentially incorrect.
>
> Further on amendment page 6 the Applicants contended that Tonnel provided no verbal description relative to the claimed depth relationships, notwithstanding the fact that we have demonstrated that Tonnel provided ample verbal description of the process of manufacture of a device that obviously possesses all the presently claimed characteristics.

Applicants respectfully submit that the Examiner is in error. While Tonnel's Figures 10-12 each show a semiconductor structure having a P-type region 22 being drawn deeper into the substrate 21 than V-slots 31, there is no corresponding verbal teaching in Tonnel's specification regarding this spatial relationship between V-slots 31 and P-type region 22. In other words, the Examiner merely speculates from hindsight that:

> ...Figures 4 through 12, combined with the corresponding written disclosure, <u>plausibly</u> demonstrated deep base regions (22), first introduced in the process step of Figure 4, <u>plausibly</u> grew deeper during the thermal oxidation step of Figure 5, at about the same depth as grooves (30) of Figure 6, and <u>plausibly</u> grew still further deeper than the depth of the grooves during ion implantation and annealing steps

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> subsequently performed in the process steps of Figures 9 and 10.
>
> (emphasis added)

The Examiner's speculation and hindsight reconstruction cannot supplement the absence of teaching in Tonnel regarding the spatial relationship discussed above and recited in Applicants' claims. Further, as amended, Claim 17 recites:

> ... wherein breakdown in said trench DMOS transistor occurs across said epitaxial layer at a position closer to said second location than said first location.

Thus, Claim 17 recites a limitation regarding the breakdown characteristics of the trench DMOS transistor resulting from the aforementioned spatial relationship. Such breakdown characteristics are neither disclosed nor suggested by Tonnel, Ueda et al., Lisiak et al., Yamabe et al., or any combination of their teachings. Similarly, independent Claims 30, 32, 46, 52 and 54 each also recite breakdown characteristics neither disclosed nor suggested by Tonnel, Ueda et al., Lisiak et al., Yamabe et al., or any combination of their teachings. Thus, Applicants believe that the various rejections under 35 U.S.C. § 103 (referenced above) by the Examiner are overcome.

As previously stated, Applicants will provide a terminal disclaimer to overcome the Examiner's obviousness-type double-patenting rejection upon the Examiner's indication of allowable subject matter otherwise.

For the foregoing reasons, Applicants believe that all claims (i.e. Claims 17-23, 25-42, 44 and 46-65) are allowable and thus respectfully request their allowance. If the Examiner has any questions regarding the above, the Examiner is

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respectfully requested to telephone the undersigned Attorney for Applicants at 408-453-9200.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on May 5, 1997.

5/5/97 Date of Signature

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